REMARKS/ARGUMENTS

In the Office Action mailed March 13, 2008, claims 1-11 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are canceled.

For reference, claims 1, 8, and 11 are amended. In particular, claims 1 and 8 are each amended to recite first and second physical banks of memory modules. These amendments are supported, for example, by the illustrations of Figs. 1 and 2, as well as the corresponding subject matter described at page 5, lines 12-20, of the specification. Claim 11 is amended to refer to remapping at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules. This amendment is supported, for example, by the subject matter described at page 8, lines 24-27, of the specification.

Claims 12-18 are added. Claims 12 and 16 recite DRAM modules. These amendments are supported, for example, by the subject matter described at page 5, lines 12-20, of the specification. Claims 13 and 17 are added to refer to remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules. These amendments are supported, for example, by the subject matter described at page 8, lines 24-27, of the specification. Claim 18 is added to refer to remapping at least one of the memory modules to a new way and a different index within the second physical bank of memory modules. This amendment is supported, for example, by the subject matter described at page 8, lines 24-27, of the specification. Claim 14 is added to refer to performing the unrestricted remapping on the basis of a reduction mapping using less output symbols than input symbols. This amendment is supported, for example, by the original language of claim 4, as well as the subject matter described at page 7, lines 1-2, of the specification. Claim 15 is added to refer to marking faulty memory modules in a look up table. This amendment is supported, for example, by the original language of claim 7

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, 5, and 7-11 were rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al. (U.S. Pat. No. 5,584,002, hereinafter Emma). Additionally, claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Asher (U.S. Pat. No. 6,671,822, hereinafter Asher). Additionally, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer). However, Applicants respectfully submit that these claims are patentable over Emma, Asher, and Kramer for the reasons provided below.

Independent Claim 1

Claim 1 recites "remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules" (emphasis added).

The specification of the present application describes a cache such as a level 2 (L2) cache for use with one or more processors. Page 5, lines 3-11; Fig. 1. The L2 cache is partitioned into several (e.g., 8) banks, which are referred to as a shared L2 cache, L2_bank. Id. Each bank can serve a read or write request independently from the other banks. Page 5, lines 12-20. This independence means that there can be concurrent transfers for each of the 8 banks. Id. Each bank is partitioned in six ways. Id. Only one way can be active in a bank at a given time. Id. Thus, the specification provides some description that illustrates how the banks are partitions of, for example, the L2 cache. Moreover, the banks have a specific relationship with the L2 cache and the ways partitions implemented in each bank. Additionally, a specific signal (i.e., the bank_select signal) is used for selecting one of the several banks. Page 6, lines 24-25.

Also, the banks recited in the claims of the present application refer to physical devices—a first physical bank of memory modules and a second physical bank of memory modules. In particular, the banks and memory modules of the L2 cache are described as being connected to a cache controller and a coherent interconnection network (CIN) for connection to other hardware such as the processing units (TM) and

the controller (DDR_ctrl). Additionally, the specification of the present application explains that the L2 cache, which includes the partitioned banks and memory modules, may be implemented as embedded dynamic random access memory (DRAM) modules. Thus, the references to banks in claim 1 refer to physical components.

In contrast to the indicated limitation of claim 1, Emma does not disclose remapping memory modules from one physical bank to another physical bank of memory modules. Emma merely addresses the historic cache synonym problem in which address references within a cache synonym class ambiguously reference addresses which have the same non-translatable address field but different translatable address bits. Emma, col. 2, line 63, through col. 3, line 9. More specifically, Emma describes a cache system to remap data in response to a hardware failure that disables a congruence class. Emma, col. 3, lines 54-59. A congruence class simply identifies a limited group of locations in the cache at which data from a given memory address may be stored. Emma, col. 1, lines 39-42. In particular, each row within the cache forms a congruence class. Emma, col. 1, lines 61-63.

Emma further explains that the loss of a single storage element in a set associative cache only disables one set of the congruence class. Emma, col. 2, lines 46-48. Additionally, Emma explains that it is possible to increase the number of congruence classes without changing set associativity. Emma, col. 2, lines 53-56. This description illustrates that the congruence classes are merely logical designations, rather than physical components within the cache. Hence, the congruence classes of Emma are not first and second physical banks, as recited in the claim, because the congruence classes are merely logical designations and are not physical banks of memory modules within the cache.

Therefore, Emma does not disclose all of the limitations of the claim because the logical congruence classes in Emma are not physical banks of memory modules. Accordingly, Applicants respectfully submit claim 1 is patentable over Emma because Emma does not disclose all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is patentable over Emma at least for similar reasons to those stated above in regard to the rejections of independent claim 1. In particular, claim 8 recites "performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules" (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1, and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejections of claim 1 also apply to the rejections of claim 8. Accordingly, Applicants respectfully assert claim 8 is patentable over Emma because Emma does not disclose remapping memory modules between physical banks of memory modules, as recited in the claim.

Dependent Claims

Claims 2-7 and 9-18 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8. Applicants respectfully assert claims 2-7 and 9-18 are allowable based on allowable base claims. Additionally, each of claims 2-7 and 9-18 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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